STATE-PRESERVING INTERMITTENTLY-LOCKED LOOP (SPILL) FREQUENCY SYNTHESIZER FOR PORTABLE RADIO

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ABSTRACT

A novel PLL concept, SPILL, suitable for intermittent-operation frequency synthesizers used in UHF portable radio sets is proposed. The SPILL employs digital circuit techniques which preserve frequency and phase during power-off periods, in order to perform fast acquisition at the beginning of power-on period. Both theoretical analysis and experiments confirm acceptable acquisition performance. A 1.6 GHz SPILL frequency synthesizer achieves two order magnitude improvement on acquisition time. Application of the SPILL to high frequency synthesizer are especially effective for reducing power consumption in the portable radio communication set.

1. INTRODUCTION

In mobile radio communications, reducing power consumption in the UHF portable radio communication set is one of the most important subjects [1],[2]. This paper focuses on power saving by intermittent operation of the phase-locked-loop (PLL) frequency synthesizer which has the highest power consumption rate in the receiver circuit. To further reduce power consumption by intermittent operation, extreme fast frequency acquisition at the beginning of the power-on stage must be realized. For this purpose, a novel PLL concept, state-preserving intermittently-locked loop (SPILL) which preserves the state (phase and frequency) of the PLL during the power-off stage, is proposed. Performance of the SPILL frequency synthesizer in 1.6 GHz band is shown theoretically and confirmed experimentally. The intermittent experiments demonstrate a very short frequency acquisition time of less than one milli-second, and extremely small frequency fluctuation. Consequently, power wasted in intermittent operation is very small, and this synthesizer has the great advantage of significantly reduced power consumption.

2. PRINCIPLE OF SPILL

A. Intermittent Operation

General control sequence of intermittent operations against a transmitted multiplexed paging signal from a base station is shown in Fig. 1. Only during periods when the required information is transmitted in the paging signal is power supplied to the receiver. For UHF band applications, it takes several tens of milliseconds for phase lock establishment after power-on. Consequently, power should be supplied earlier by a time equivalent to this phase lock establishment. For intermittent operation, phase lock establishment time should be much shorter than power-on period to increase the effectiveness of power reduction.

B. Principle of SPILL

The state of the PLL can be represented by its phase and frequency. In the SPILL synthesizer, if its states of phase and frequency are preserved during the power-off stage, at the beginning of the power-on stage, the previous PLL states are recovered in a very short time without frequency fluctuation.

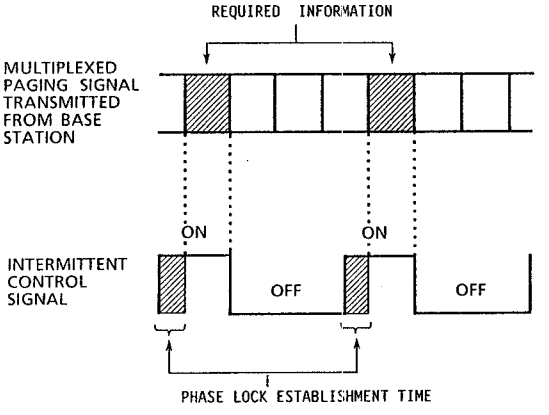

Fig. 1 Control sequence of intermittent operation.

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In practical intermittent operation, frequency preservation during power-off stage can be performed by interrupting the phase difference voltage from the phase comparator to the VCO. To preserve the phase, a new "initial-phase adjustment" technique is proposed. This technique enables the phase difference at the beginning of power-on stage is adjusted within one period of the UHF band VCO signal. Further information about these techniques will be given in section III.

C. Analysis of phase lock process in SPILL

If, after the loop is closed, there is an extremely small phase difference for the initial-phase adjustment, it is assumed that the phase locking process can be investigated as a frequency stepping response or a phase stepping response [3]. In this analysis, frequency transitional profiles at phase or frequency

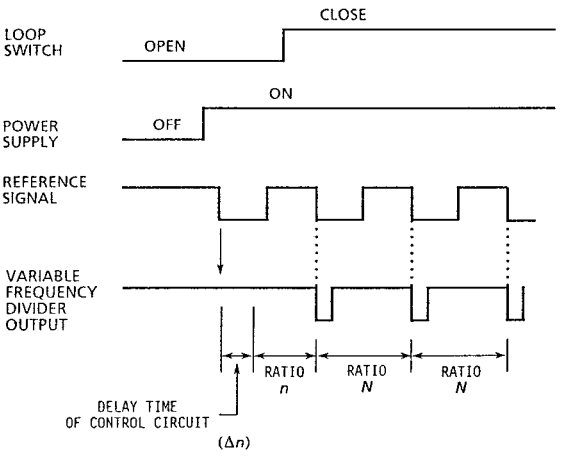

Fig. 4 Timing sequence of the newly developed initial phase adjustment circuit.

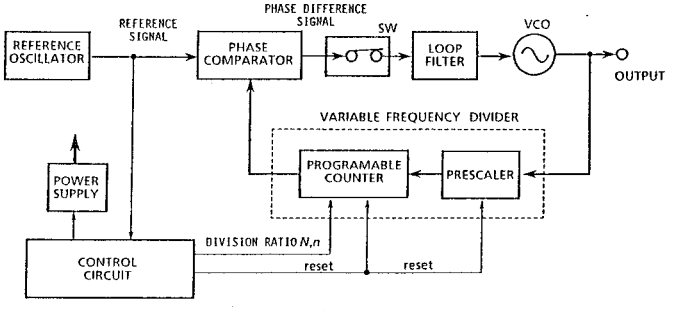

Fig. 2 A SPILL frequency synthesizer using a newly developed initial phase adjustment technique.

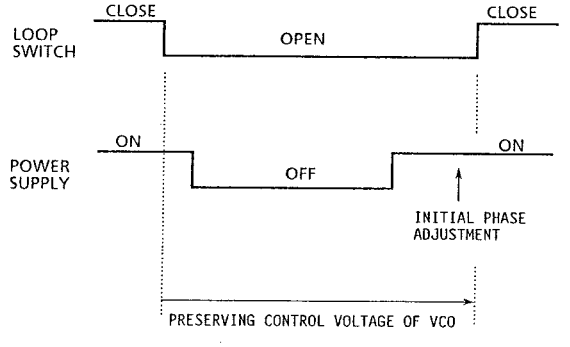

Fig. 3 Control sequence of intermittent operation.

stepping response and phase lock establishment time are simulated.

The feedback circuit used in this investigation is composed of a digital type of phase comparator, a lag-lead type loop-filter, and a current source chargepump whose output has 3 states, charge, discharge and open. Therefore, the phase locking process is identified by PLL behavior which uses a fully-integrated filter.

The analysis of frequency stepping response showed that, when the initial frequency difference is less than 100 Hz at VCO output frequency, the deviation of frequency fluctuation after loop closure becomes gradually zero without a large frequency fluctuation.

Furthermore, in the case of phase stepping response, when the initial phase difference is less than $5 \times 10 - 5$ radian, the deviation of frequency fluctuation after the loop is closed becomes less than 100 Hz, and its phase lock establishment time is about 1 millisecond.

3. INITIAL PHASE ADJUSTMENT TECHNIQUE

A SPILL frequency synthesizer using a newly developed initial-phase adjustment technique, and its control sequence are shown in Fig.2, and Fig.3, respectively. This frequency synthesizer uses a resettable variable frequency divider, instead of a conventional one for dividing the VCO signal. Operations of this circuit consist of : (1) basic phase adjustment operation and (2) precise phase adjustment.

A. Basic Phase Adjustment Operation

First, a switch is opened to maintain control voltage of the loop filter. Then, each circuit is put in the power-off state for a specified period. Then the variable frequency divider is reset to initialize the pulse count state. In this way, the divider is prepared to count from the initial state at the next divide

operation. Power to each circuit is supplied again after a certain period of power-off state. Next, just before closing the loop, the count operation of the reset variable frequency divider is started, synchronously with the edge of the reference signal. If this phase adjustment is completed, it is possible to match phases to a precision of one period of VCO output signal.

However, there are several tens of nanoseconds delay in the control circuit above, and this is added to phase difference.

B. Precise Phase Adjustment

To remove the delay time mentioned above, the division ratio of the variable frequency divider is controlled at two stages when it starts the count operation (refer to Fig. 4). The division ratio of n is used only in the first period of count operation of the variable frequency divider. The ratio n is obtained by subtracting division ratio Δn, which corresponds to the delay time, from normal division ratio N which determines the channel. Phase difference resulting from the delay time can be removed by this procedure. Furthermore, normal division ratio N which determines the channel is set in the second and later count operations. It is possible to adjust phase difference precisely by a period of VCO output signal, according to the selected value n. When this technique of controlling a division ratio is used, the maximum phase difference will be approximately $5 \times 10 - 5$ radian for the 1.6 GHz band frequency synthesizer at 12.5 kHz reference signal.

4. CHARACTERISTICS OF THE INTERMITTENT OPERATION

A. Experimental Circuits

In the experiment, a 1.6 GHz band frequency synthesizer was used. It consisted of a VCO generating a 1.6 GHz signal directly and a PLL circuit with a resettable variable frequency divider. The resettable variable frequency divider constituted a pulse swallow counter with a resettable prescaler (256/258) and a programable counter. The resettable prescaler integrated circuit was newly developed through NTT's Si process [4].

B. Intermittent Operation

Fig. 5 shows VCO output frequency fluctuation when the power supply of PLL circuit including VCO is in the intermittent operation mode. Frequency deviation was measured using a spectrum analyzer, whose sweep span was made 0 Hz, as a frequency discriminator. The division ratio n of the variable frequency divider at its first period was adjusted to $n = N - 18$.

Frequency became stable within only 1 ms using the initial phase adjustment as shown in Fig. 5 where previously it used to take about 150 ms, and the frequency fluctuation during power-on period could not be detected. These results are in good agreement with theoretical estimations. Therefore, it is not necessary to supply extra power for phase

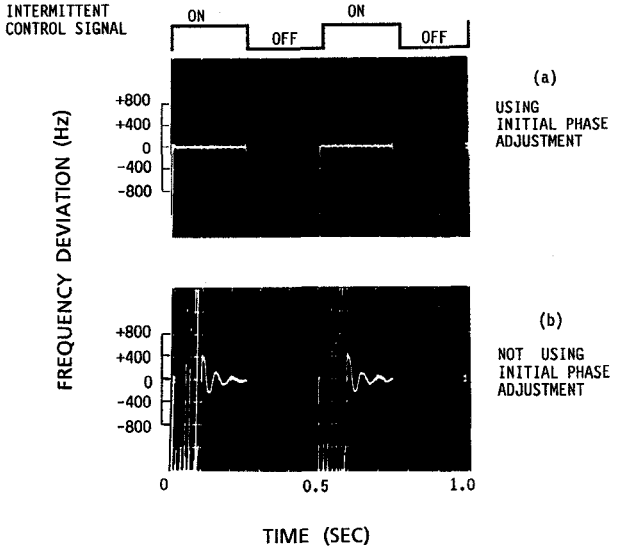

Fig. 5 VCO output frequency fluctuation when power supply of PLL circuit including VCO, is in the intermittent operation with 1.6 GHz frequency synthesizer.

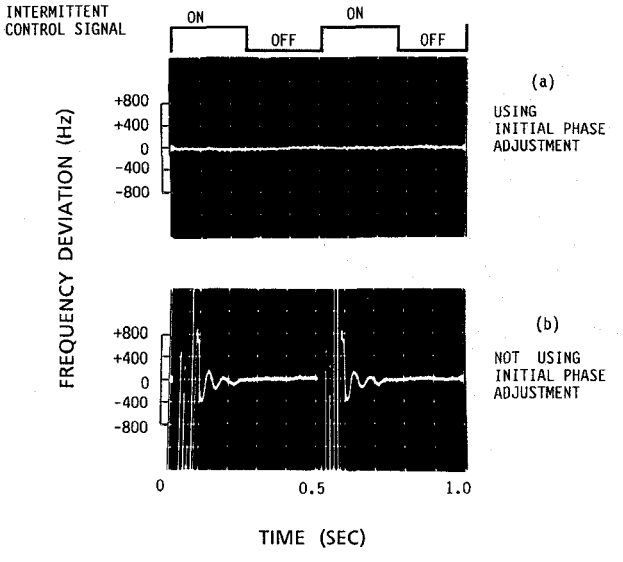

Fig. 6 VCO output frequency fluctuation when VCO is kept in the power-on state and the power supply of PLL circuit is in the intermittent operation with 1.6 GHz frequency synthesizer. The ratio of ON/OFF is 1.

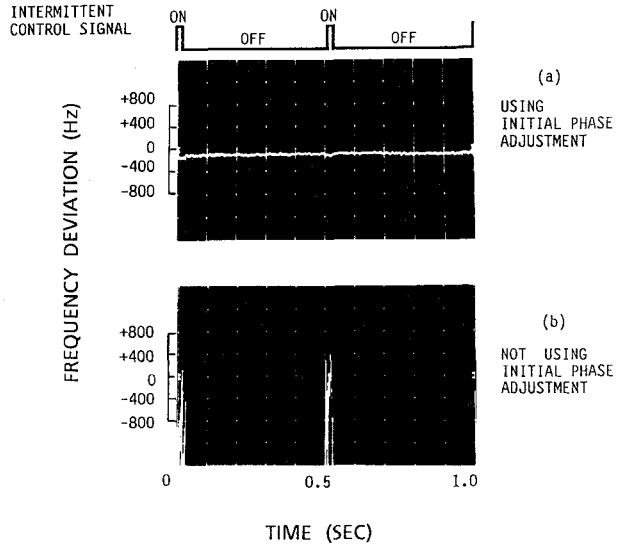

Fig. 7 VCO output frequency fluctuation when VCO is kept in the power-on state and the power supply of PLL circuit is in the intermittent operation. The ratio of ON/OFF is 1/19.

locking each intermittent period, and during each entire power-on period, the synthesizer's output is available as a stable signal. These results show that using the initial phase adjustment is more effective for reducing synthesizer's power consumption than just intermittent operation.

If SPILL is applied to NTT 's high capacity land mobile communication systems [1], the usage time of a portable battery telephone will be increased 1.5 times.

For other transceiver systems, Fig.6 shows VCO output frequency fluctuation when VCO is kept in the power-on state and the power supply of other PLL circuits is in the intermittent operation mode. As shown in this figure, if the initial phase adjustment is used, the PLL circuit can be operated intermittently with little frequency fluctuation. The ratio of ON/OFF in the intermittent operation can be 1/19 or less as shown in Fig.7. Therefore, power consumption of the PLL circuit, including the prescaler,is expected to be reduced to 1/20 or less. Selection of a capacitor with small leakage is likely to minimize power consumption. It is very difficult to achieve the reduced power consumption described above using advanced high-speed semiconductor integrated circuits only.

5. CONCLUSION

A state-preserving intermittently-locked loop (SPILL) frequency synthesizer using a resettable variable frequency divider suitable for intermittent operation to reduce power consumption, has been developed.

This frequency synthesizer is effective in reducing the power consumption of land mobile communication systems and many kinds of communication systems using radio equipment with high-band frequency synthesizer, such as portable TVs, cordless phones, paging systems, satellite communications and terrestrial microwave communications. Besides, an application of the initial phase adjustment will be also available for fast frequency switching.

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